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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,694	03/05/2002	Bruce E. Lavigne	100202225-1	7434

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EXAMINER	
ABELSON, RONALD B	
ART UNIT	**PAPER NUMBER**
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/091,694	LAVIGNE ET AL.	
	Examiner	Art Unit	
	Ronald Abelson	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-10,12,15-19 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-10,12,15-19 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/23/07 and 3/5/02* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4, 5, 8, 19, and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCloghrie in view of Demars (US 7,088,739) and Davidson (US 6,550,002).

Regarding claims 1, 19, and 23, McCloghrie teaches a processor (fig. 1 box 120, col. 3 lines 31-34) connected to a network device (fig. 1 box 110).

McCloghrie teaches an input interface for receiving a plurality of packets coupled to the processor (fig. 1 element 111, col. 3 lines 31-34), the input interface comprising at least one input port wherein at least one said input port is configured to sample at least one input packet and transmit a sampled input packet to the processor (fig. 1 box 111, sampling of packets occurs at input interfaces 111, forwards sampled

packets to another portion of traffic management element 120, col. 3 lines 42-52), wherein at least one said input port comprises a sampling device, wherein said input port is configured to sample a packet according to said sampling device (fig. 1 box 111, sampling of packets occurs at the input interfaces, col. 3 lines 42-45, sample one out of every N packets, col. 4 lines 41-43).

McCloghrie teaches an output interface for transmitting a plurality of packets coupled to the processor (fig. 1 element 112, col. 3 lines 31-34), the output interface comprising at least one output port wherein at least one said output port is configured to sample at least one output packet and transmit a sampled output packet to the processor (fig. 1 box 112, sampling of packets occurs at output interfaces 112, forwards sampled packets to another portion of traffic management element 120, col. 3 lines 42-52), wherein said input interface and said output interface feed into said processor (traffic management element 120 is coupled to substantially all input interfaces and substantially all output interfaces, col. 3 lines 31-41), wherein at least one said output port comprises a sampling device, wherein said output port is configured to sample a packet according to said sampling device (fig. 1 box 112, sampling of packets occurs at the output interfaces, col. 3

lines 42-45, sample one out of every N packets, col. 4 lines 41-43).

McCloghrie teaches a switching fabric coupled to the input interface and the output interface, the switching fabric configured to transmit a packet between the input interface and output interface (fig. 1 box 110, col. 3 lines 22-29).

Regarding claims 19 and 23, in addition to the limitations previously addressed, a plurality of input means (fig. 1 boxes 111) and output means (fig. 1 boxes 12).

Regarding claim 23, in addition to the limitations previously addressed, a computer-readable memory coupled to said input interface and said output interface (fig. 1 box 130, col. 4 lines 1-5) and a microcontroller coupled to said input interface and said output interface, said microcontroller for executing a method of sampling a packet (fig. 2 Sampling CTRLR, col. 4 lines 19-21).

Although McCloghrie teaches a processor (fig. 1 box 120) that performs sampling and a network device / switch (fig. 1 box 110), the reference does not explicitly teach the processor is CPU integrated with the network device (fig. 1 box 110).

Demars teaches a processor / CPU integrated within the network device / switch (fig. 3A box 300, 304, fig. 6A box 600, 612, col. 5 lines 1-5, col. 6 lines 44-47).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of McCloghrie by incorporating the processor (fig. 1 box 120) within the network device (fig. 1 box 110). This modification can be performed according to the teachings of Demars. This modification would benefit the system by allowing for all the functions to be performed on a single, reliable, inexpensive device.

Although the combination teaches at least one input and output port comprising a sampling device, wherein said input and output ports are configured to sample a packet according to said sampling device, the combination does not explicitly teach each input and output port comprises a countdown register.

Davidson teaches a countdown register (monitoring countdown register for value of zero, col. 12 lines 30-32).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination by keeping track of when the Nth packet occurs to be sampled at the input and output ports by using a countdown register at each port, as suggested by Davidson. This modification can be

performed according to the teachings of Davidson. This modification would benefit the system since countdown registers are cheap, reliable devices for determining when a periodic event has occurred.

Regarding claims 4 and 22, the CPU (McCloghrie: fig. 1 box 120, fig. 2 box 120) transmits said sampled input packet and said sampled output packet to a central control station (fig. 2 see transmission of packet from box 250 to 260; col. 5 lines 62-65) over a network. The Examiner corresponds applicant's central control station with the Type Detector and Frequency Measure (fig. 2 box 260, 270) of the reference and the applicant's network with the connection from box 250 to 260 in the reference.

Regarding claim 5, the central control station comprises a statistical monitoring station (fig. 2 box 270, col. 6 lines 8-13).

Regarding claim 8, the network comprises a local area network (McCloghrie: see connection from box 120 to 130). Note,

examiner corresponds to connection from boxes 120 to 130 to be via a LAN.

Regarding claims 24 and 25, the microcontroller transmitting said sampled incoming/outgoing packet to a statistical monitoring station (fig. 2 box 270) over a network (see the connection from box 250 to 260).

3. Claims 10, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCloghrie in view of Genrich (US 5,596,609), and Schueler (US 5,682,034).

Regarding claim 10, McCloghrie teaches for receiving a plurality of packets at an input network circuit, said input network circuit comprising at least one input port (fig. 1 element 111, col. 3 lines 31-34).

McCloghrie teaches sampling at least one input packet, wherein said sampling comprises using a sampling device (fig. 1 box 111, sampling of packets occurs at input interfaces 111, sample one out of every N packets, col. 4 lines 41-43)

McCloghrie teaches transmitting at least one sampled input packet to a processor (forwards sampled packets to another portion of traffic management element 120, col. 3 lines 42-52).

McCloghrie teaches transmitting at least one packet from said network circuit to an output network circuit (fig. 1: see output of box 120 to box 130) over a switching fabric (fig. 1 box 110), said output network circuit comprising a plurality of output ports (fig. 1 boxes 112), wherein said input network circuit and said output network circuit feed into said processor.

McCloghrie teaches sampling multiple output packets simultaneously at said plurality of output ports (fig. 1 see connection from output ports 112 to box 120).

McCloghrie teaches transmitting at least one packet from said input network circuit to an output network circuit of said network device over a switching fabric of said network device, said output network circuit comprising at least one output port (fig. 1 see connection from port 111 to port 112 through router/switch box 110) wherein said input network circuit and said output network circuit feed into said processor (traffic management element 120 is coupled to substantially all input interfaces and substantially all output interfaces, col. 3 lines 31-41).

Although McCloghrie teaches a processor (fig. 1 box 120) that performs sampling, the reference does not explicitly the processor is integrated with the network device (fig. 1 box 110).

Genrich teaches a network device / integrated circuit capable of performing the sampling functions listed above (integrated circuit, sampling rate, col. 3 lines 39-42).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of McCloghrie by incorporating the sampling functions (fig. 1 box 120) on a single integrated circuit within the router/switch (fig. 1 box 110). This modification can be performed according to the teachings of Genrich. This modification would benefit the system by allowing for all the functions to be performed on a single, reliable, inexpensive device.

Although the combination teaches sampling multiple output packets simultaneously at the plurality of output ports, the combination is silent on countdown circuits, wherein each of the plurality of output ports comprises one of the countdown circuits.

Schueler teaches sampling using countdown circuits (col. 4

lines 43-45).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination by keeping track of when the Nth packet occurs to be sampled at each input and output port by using a countdown circuit at each port, as suggested by Schueler. This modification would benefit the system since countdown registers are cheap, reliable devices for determining when a periodic event has occurred.

Regarding claim 15, the processor (McCloghrie: fig. 1 box 120, fig. 2 box 120) transmitting said sampled input packet (fig. 1,2 box 120, col. 5 lines 62-65) to a statistical monitoring station (fig. 2 box 270, col. 6 lines 8-13) over a network (see connection from box 250 to 260).

Regarding claim 16, the processor (McCloghrie: fig. 1 box 120, fig. 2 box 120) transmitting said sampled multiple output packets (fig. 1,2 box 120, col. 5 lines 62-65) to a statistical monitoring station (fig. 2 box 270, col. 6 lines 8-13) over a network (see connection from box 250 to 260).

4. Claim 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of McCloghrie, Demars, and Davidson as applied to claim 1 above, and further in view of Dean (US 6,442,585).

Regarding claim 9, although the combination teaches a countdown register, the reference is silent on a random number countdown register.

Dean teaches a random number countdown register (fig. 2 box 265, countdown register, random sampling, col. 7 lines 31-37).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination by replacing the countdown registers at the input and output ports with a random number countdown register as suggested by Dean. This modification would benefit the system by providing for improved statistical sampling.

5. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of McCloghrie, Demars, and Davidson as applied to claim 1 above, and further in view of Chen (US 6,658,006).

Regarding claim 6, the combination is silent on the sampled input packet comprises an identification of the input port that sampled the sampled input packet.

Chen teaches a method for modifying the header bits of an incoming packet to identify the input port (col. 1 lines 48-51).

Regarding claim 7, the combination is silent on the sampled output packet comprises an identification of the output port that sampled the sampled input packet.

Chen teaches a method for modifying the header bits of a packet to identify the output port (col. 1 lines 51-55).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination by incorporating within the input and output ports logic to modify the header bits to identify the respective input/output ports. This modification can be performed according to the teachings of Chen. This information could be useful in load balancing.

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of McCloghrie, Genrich, and Schueler as applied to claim 10 above, and further in view of Chen (US 6,658,006).

Regarding claim 17, the combination of McCloghrie and Genrich is silent on the sampled input packet comprises an identification of the input port that sampled the sampled input packet.

Chen teaches a method for modifying the header bits of an incoming packet to identify the input port (col. 1 lines 48-51).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination by incorporating within the input and output ports logic to modify the header bits to identify the respective input/output ports. This modification can be performed according to the teachings of Chen. This information could be useful in load balancing.

7. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of McCloghrie, Genrich, and Schueler as applied to claim 10 above, and further in view of Chen (US 6,658,006) and Westphal (6,651,052).

Regarding claim 18, the combination of McCloghrie and Genrich is silent on the sampled output packet comprises an identification of the output port that sampled the sampled input packet.

Chen teaches a method for modifying the header bits of a packet to identify the output port (col. 1 lines 51-55).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination by incorporating within the input and output ports logic to modify the header bits to identify the respective input/output ports. This modification can be performed according to the teachings of Chen. This information could be useful in load balancing.

The combination is silent on a bitmap.

Westphal teaches a bitmap (col. 1 lines 63-64).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination by storing the information in a bitmap, as suggested by Westphal. This modification can be performed in software. This modification would benefit the system since a bitmap provides efficient memory usage (Westphal: col. 1 lines 63-64).

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of McCloghrie, Genrich, Schueler as applied to claim 10 above, and further in view of Dean (US 6,442,585). Note: since random number countdown circuit

is not a term of art, the examiner assumes the applicant is referring to a random number countdown register.

Although McCloghrie teaches a countdown register, the combination is silent on a random number countdown register.

Dean teaches a random number countdown register (fig. 2 box 265, countdown register, random sampling, col. 7 lines 31-37).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination of McCloghrie and Genrich by replacing the countdown registers at the input and output ports with a random number countdown register as suggested by Dean. This modification would benefit the system by providing for improved statistical sampling.

Response to Arguments

9. Applicant's arguments with respect to amended claims have been considered but are moot in view of the new ground(s) of rejection.

Regarding claim 1, applicant's contention that the combination of McCloghrie and Genrich does not teach a CPU (applicant: pg. 10 first paragraph), this issue has been addressed in the office action. Regarding the countdown register

(applicant: pg. 10 first paragraph), this issue is addressed in the office action.

Regarding claim 10, applicant's contention that the combination of McCloghrie and Genrich does not teach a plurality of countdown circuits (applicant: pg. 11 2nd paragraph), this issue is addressed in the office action.

Regarding claim 19, applicant's contention that the combination of McCloghrie and Genrich does not teach a countdown means (applicant: pg. 12 last paragraph), this issue is addressed in the office action.

Regarding claim 23, applicant's contention that the combination of McCloghrie and Genrich does not teach a countdown register (applicant: pg. 14 1st paragraph), this issue is addressed in the office action.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is

reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald Abelson whose telephone number is (571) 272-3165. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (571) 272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ronald Abelson
Examiner
Art Unit 2616

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CHI PHAM
SUPERVISORY PATENT EXAMINER 6/5/07